IN THE SPECIFICATION:

Please replace the paragraph beginning at line 24 of page 1 with the following rewritten paragraph:

b1

-- One of the rendering methods is polygon rendering. In this method, a three-dimensional model is expressed as a composite of triangular unit graphics (polygons). By drawing the polygons as units, the colors of the pixels of the display screen are decided. --

Please replace the paragraph beginning at line 17 of page 26 with the following rewritten paragraph:

b2

-- The operation sub-blocks 203_1 to 203_8 perform the above blending and output the (R, G, B, α) data $S203_1$ to $S203_8$ only when results of the level detection of the val data $S220_1$ to $S220_8$ by the clock enablers 213_1 to 213_8 are "1." --

Please replace the paragraph beginning at line 23 of page 26 with the following rewritten paragraph:

b3

-- The operation block 204 has the operation sub-blocks 204_1 to 204_8 and performs a z-comparison for the input (R, G, B, α) data $S203_1$ to $S203_8$ by using the content of the z-data stored in the z-buffer 22. When the image drawn by the (R, G, B, α) data $S203_1$ to $S203_8$ is positioned closer to the viewing point than the image drawn in the display buffer 21 the previous time, the operation block 204 updates the z-buffer 22 and

outputs the (R, G, B, α) data $S203_1$ to $S203_8$ as the (R, G, B, α) data $S204_1$ to $S204_8$ to the operation sub-blocks 205_1 to 205_8 of the operation block 205. --

Please replace the paragraph beginning at line 15 of page 27 with the following rewritten paragraph:

-- The operation block 205 has the operation sub-blocks 205_1 to 205_8, blends the (R, G, B, α) of the data $S204_1$ to $S204_8$ and the (R, G, B) data already stored in the display buffer 21 by the blending ratio indicated in the α data included in the (R, G, B, α) data $S204_1$ to $S204_8$, and writes the blended (R, G, B) data $S205_1$ to $S205_8$ in the display buffer. --

Please replace the paragraph beginning at line 25 of page 29 with the following rewritten paragraph:

-- Here, a case of, for example, simultaneous processing on 8 pixels in a block 31 shown in Fig. 12 will be considered. In this case, the val data $S220_1$, $S220_2$, $S220_3$, $S220_5$, and $S220_6$ indicate "0" and the val data $S220_4$, $S220_7$, and $S220_8$ indicate "1." --

Please replace the paragraph beginning at line 8 of page 30 with the following rewritten paragraph:

-- Then in the clock enablers 210_1 to 210_8, the levels of the respective val data

$S220_1$ to $S220_8$ are detected. Specifically, "1" is detected in the clock enablers 210_4, 210_7, and 210_8 and "0" is detected in the clock enablers 210_1, 210_2, 210_3, 210_5, and 210_6. --

Please replace the paragraph beginning at line 25 of page 30 with the following rewritten paragraph:

B7 -- Next, the clock enablers 211_1 to 211_8 of the operation sub-blocks 201_1 to 201_8 detect the levels of the respective val data $S220_1$ to $S220_8$. --

Please replace the paragraph beginning at line 10 of page 31 with the following rewritten paragraph:

B8 -- On the other hand, no operation is performed in the operation sub-blocks 201_1, 201_2, 201_3, 201_5, and 201_6. --

Please replace the paragraph beginning at line 8 of page 32 with the following rewritten paragraph:

B9 -- Next, the clock enablers 213_1 to 213_8 of the operation sub-blocks 203_1 to 203_8 detect the levels of the respective val data $S220_1$ to $S220_8$. --

Please replace the paragraph beginning at line 11 of page 32 with the following rewritten paragraph:

B10 -- Then, based on the detection results, only the operation sub-blocks 203_4, 203_7,

B10 and 203_8 blend the texture data (R, G, B, α) $S202_4$, $S202_7$, and $S202_8$ input from the operation block 202 and the (R, G, B) data included in the DDA data S11 from the triangle DDA circuit 11 by the blending ratio indicated by the α data (texture α) included in the (R, G, B, α) data $S202_4$, $S202_7$, and $S202_8$ to generate the blended data (R, G, B). --

Please replace the paragraph beginning at line 14 of page 36 with the following rewritten paragraph:

B11 -- Here, the DDA set-up circuit 10, the texture engine circuit 12, the CRT controller circuit 14, the RAMDAC circuit 15, the DRAM 16, and the SRAM 17 are the same as those explained in the first embodiment. --

Please replace the paragraph beginning at line 6 of page 44 with the following rewritten paragraph:

B12 -- The operation block 500 has operation sub-blocks 501_1 to 500_8 and receives as input the DDA data S11 from the triangle DDA circuit 11 shown in Fig. 7. --

Please replace the paragraph beginning at line 9 of page 44 with the following rewritten paragraph:

B13 -- The operation sub-blocks 501_1 to 500_8 detect the levels of the val data $S220_1$ to $S220_8$ included in the DDA data S11 in the respective clock enablers 510_1 to 510_8 and

B13

perform the z-comparison when the level is "1" (when the pixel is inside a triangle being processed), while do not perform the z-comparison when the level is not "1." --

Please replace the paragraph beginning at line 6 of page 47 with the following rewritten paragraph:

B14

-- The operation block 503 has operation sub-blocks 503_1 to 503_8, outputs a read request including the texture coordinate data (u, v) generated in the operation block 502 to the SRAM 17 or DRAM 16 via the memory I/F circuit 13, and reads the texture data stored in the SRAM 17 or the texture buffer 20 via the memory I/F circuit 513 to obtain the (R, G, B, α) data S17 stored in the texture address corresponding to the (u, v) data. --

Please replace the paragraph beginning at line 7 of page 49 with the following rewritten paragraph:

B15

-- First, the clock enablers 510_1 to 510_8 of the operation sub-blocks 500_1 to 500_8 detect the levels of the val data $S220_1$ to $S220_8$ included in the DDA data S11. When the detected level is "1" (when the pixel is inside the triangle being processed), the z-comparison is performed. --

Please replace the paragraph beginning at line 2 of page 52 with the following rewritten paragraph:

-- Next, in the clock enablers 515_1 to 515_8 of the operation sub-blocks 505_1 to 505_8, the levels of the val data $S220_1$ to $S220_8$ and $S500a_1$ to $S500a_8$ are detected. Only when both of the levels are "1," the (R, G, B, α) data $S504_1$ to $S504_8$ and the (R, G, B) data already stored in the display buffer 21 are blended by the blending ratio indicated by the α data included in the respective (R, G, B, α) data $S504_1$ to $S504_8$. The blended (R, G, B) data $S505_1$ to $S505_8$ are written in the display buffer 21. --

B16

Please replace the paragraph beginning at line 5 of page 53 with the following rewritten paragraph:

-- For example, in the above second embodiment, as shown in Fig. 6, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 12 and the memory I/F circuit 413. However, as shown in Fig. 9, 1 pixel of data may be processed in the operation blocks as well. --

B17

Please replace the paragraph beginning at line 18 of page 53 with the following rewritten paragraph:

-- Also, in the above third embodiment, as shown in Fig. 8, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 512 and the memory I/F circuit 513. However, as shown in

B18